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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
SURYAWANSHI, SURESH	
ART UNIT	**PAPER NUMBER**
2115	

DATE MAILED: 04/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/981,474	TESTER, DAVID P.	
	Examiner	Art Unit	
	Suresh K. Suryawanshi	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *3/10/05 amendments*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *21-23* is/are allowed.

6)☒ Claim(s) *1-8,11-18 and 20* is/are rejected.

7)☒ Claim(s) *9,10 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-23 are presented for examination.

Drawings

2. This application, filed under former 37 CFR 1.60, lacks formal drawings. The informal drawings filed in this application are acceptable for examination purposes. When the application is allowed, applicant will be required to submit new formal drawings. In unusual circumstances, the formal drawings from the abandoned parent application may be transferred by the grant of a petition under 37 CFR 1.182.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 20 recites the limitation "said first frequency" in lines 7-8. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1- are rejected under 35 U.S.C. 102(b) as being anticipated by Yeung et al (US Patent No 5,889,436).

7. As per claim 1, Yeung et al disclose a prescaler comprising:

a first circuit configured to generate a plurality of control signals in response to a first clock signal having a first frequency [Fig. 8; VCO 68 generates a plurality of control signals in response to a first clock signal 58 having a first frequency];

a multiplexer configured to multiplex a plurality of data signals in response to said control signals to present a second clock signal having a second frequency that is a non-integer fraction of said first frequency [Fig. 8; MUX 80 is configured to multiplex a plurality of data signals from the SR 88 in response to said control signals to present a second clock signal 78 (f_{FB}) having a second frequency that is a non-integer fraction of said first frequency; col. 3, lines 27-32]; and

a second circuit configured to (i) generate said data signals in response to said second clock signal [Fig. 8; SR 88 generates the data signals in response to second clock signal 78 (f_{FB})] and (ii) present said data signals directly to said multiplexer [Fig. 8; SR 88 presents the data directly to MUX 80].

8. As per claim 11, Yeung et al disclose a method of dividing a first clock signal having a first frequency [Fig. 8; VCO 68 divides a first clock signal 58 having a first frequency], the method comprising the steps of :

generating a plurality of control signals in response to said first clock signal [Fig. 8; VCO 68 generates a plurality of control signals in response to a first clock signal 58 having a first frequency];

multiplexing a plurality of data signals in response to said control signals to present a second clock signal having a second frequency that is a non-integer fraction of said first frequency [Fig. 8; MUX 80 is configured to multiplex a plurality of data signals from the SR 88 in response to said control signals to present a second clock signal 78 (f_{FB}) having a second frequency that is a non-integer fraction of said first frequency; col. 3, lines 27-32];

generating said data signals in response to said second clock signal [Fig. 8; SR 88 generates the data signals in response to second clock signal 78 (f_{FB})]; and

presenting said data signals directly to said multiplexing [Fig. 8; SR 88 presents the data directly to MUX 80].

9. As per claim 20, Yeung et al disclose a prescaler comprising :

means for generating a plurality of control signals in response to a first clock signal [Fig. 8; VCO 68 generates a plurality of control signals in response to a first clock signal 58 having a first frequency];

means for multiplexing a plurality of data signals in response to said control signals to present a second clock signal having a second frequency that is a non-integer fraction of said first frequency [Fig. 8; MUX 80 is configured to multiplex a plurality of data signals from the SR 88 in response to said control signals to present a second clock signal 78 (f_{FB}) having a second frequency that is a non-integer fraction of said first frequency; col. 3, lines 27-32]; and

means for generating said data signals in response to said second clock signal [Fig. 8; SR 88 generates the data signals in response to second clock signal 78 (f_{FB})].

10. As per claims 2 and 12, Yeung et al disclose that second circuit is further configured to sequence said data signals through a plurality of patterns response to said second clock signal [Fig. 8; SR 80 shifts data bits in response to the second clock signal 78 (f_{FB})].

11. As per claims 3 and 13, Yeung et al disclose that second circuit is further configured to present said data singles in a first predetermined pattern such that said second frequency is an integer fraction of said first frequency [Fig. 8; SR 80 present the data signals in a first predetermined pattern such that the second frequency is an integer fraction of said first frequency; col. 3, lines 27-32].

12. As per claims 5 and 15, Yeung et al disclose that a plurality of latches configured to latch said data signals [Fig. 8; SR 88 is a shift register].

13. As per claims 6 and 16, Yeung et al disclose that latches are further configured to sample said data signals [Fig. 8; SR 88 is a shift register].

14. As per claims 7 and 17, Yeung et al disclose that first circuit is further configured to present one of said control signals in an active state at a time [Fig. 8; VCO circuit 68].

15. As per claims 8 and 18, Yeung et al disclose that first circuit is further configured to present at least two of said control signals in an active state at a time [Fig. 8; VCO circuit 68].

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. Claims 4 and 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yeung et al (US Patent No 5,889,436).

18. As per claims 4 and 14, Yeung et al disclose the invention substantially. Yeung et al do not expressly disclose about the second frequency being equal to the first frequency. However, a routineer in the art would know to generate a second clock having a second frequency being equal to the frequency of the first clock just by sending the first clock straight to multiplexer without introducing an inverter in between of the first clock and multiplexer. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the first circuit of the invention where the first clock signal is sent to the multiplexer directly. Moreover, a routineer wants to use the first clock frequency without any inverter to cover all possible clock frequencies for shifting the data bits in the shift register and thus having one more sequence of data bit pattern.

Allowable Subject Matter

19. Claims 21-23 are allowed.

20. Claims 9, 10 and 19 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

21. Applicant's arguments with respect to claims 1-8, 11-18 and 20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suresh K. Suryawanshi whose telephone number is 571-272-3668. The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sks
April 11, 2005